REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 are rejected.

In a telephone interview with the previous Examiner, Joseph Logsdon, of November 15, 2002, the Examiner conceded that the Applicants' application was in condition for allowance. The Examiner conceded that the Applicants' claims 1-15, 18, 19, 21 and 22 were described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors had possession of the claimed invention. Specifically, the Applicants directed the Examiner's attention to the Applicants' specification on page 12 line 27 through page 13 line 27.

In view of this Final Office Action, it appears that the new Examiner was not informed by the previous Examiner of the telephone interview, nor did the previous Examiner issue a telephone interview summary, which lead to an improper Final Office Action to be issued for this application.

In this response, the Applicants are reiterating the arguments presented to the previous Examiner, Joseph Logsdon, for support of the rejected claims. For at least the reasons stated herein, which are substantially the same reasons presented to the previous Examiner in the telephone interview of November 15, 2002, the Applicants submit that all of the claims presently in the application now satisfy the requirements of 35 U.S.C. § 112. Thus, the Applicants believe that all of the claims are now in allowable form.

Objections

The Examiner has objected to claims 14 and 15 under 37 CFR 1.75(c) as being of improper dependent form for failing to further limit the subject matter of the previous claim.

In response the Applicants have amended claim 14 to depend from claim 11 to correct for the inadvertent formality error. As such, the Applicants

respectfully submit that claim 14 further limits claim 11 and satisfies the requirements of 37 CFR 1.75(c).

Furthermore, claim 15 depends from and further limits claim 14 and as such, the Applicants respectfully submit that claim 15 also satisfies the requirements of 37 CFR 1.75(c).

Therefore, the Applicants respectfully request that the Examiner's objections to claims 14 and 15 be removed.

Rejections

A. 35 U.S.C. § 112

The Examiner has rejected claims 1-15, 19, 21, and 22 under the provisions of the first paragraph of 35 U.S.C. § 112 as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, the Examiner alleges that "Claims 1, 5, 6, 11, 16, and 20 recite an apparatus and method of conveying any selected input bit pack to any output data positions and that the disclosure as originally filed does not teach this feature. As such, the Examiner rejected claims 2-4, 7-10, 12-15, 17-19 and 21-22 upon the rejection of independent claims

In accordance with and for the reasons stated in the telephone interview of November 15, 2002 and restated herein, the previous Examiner, Joseph Logsdon, had withdrawn his objections to claims 1-15, 18, 19, 21, and 22. The Examiner stated that the subject matter of claims 1-15, 19, 21, and 22 are fully described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In support of the at least claims 1, 5, 6, 11, 16, and 20, the Applicants, in the specification, specifically recite:

"In this illustrative embodiment, the first bits of 4 input channels, c1b1 through c4b1 are switched to the first bits of 4 output channels, c5b1 through c8b1. A 4 to 2 multiplexer 402, multiplexes bit-pack, first bits routed to the switching core 400 from various disassemblers, to 2 to 1 multiplexers 404, 406, 408, and 410. In this illustrative embodiment, during the first time slot, the multiplexer 402 selects bits c1b1 and c2b1 and routes those bits to 2 to 1 multiplexers 404-410. During the second time slot, the multiplexer 402 selects bits c3b1 and c4b1 and routes them to the 2 to 1 multiplexers 404-410. **In this manner, each of the 2 to 1 multiplexers 404-410 may select any input, c1b1 through c4b1 to latch into a storage area 412-418,** respectively." (See Applicants' specification, page 10, lines 3-11). (emphasis added).

"Such space/time switches may be implemented in a variety of configurations, with different combinations of rails and time slots. Figure 7 provides a conceptual block diagram of an illustrative embodiment of such a space/time implementation 700, which will be referred to hereinafter as an expander space/time switch. Such a configuration employs a selection block 701 for each of the seven hundred and sixty eight locations in the switch core's output bit map. In the illustrative embodiment, each selection block 701 employs a 32 to one multiplexer 702 to select one of 32 rails. The selected rail may remain the same in all 24 time slots 704 because control circuitry, illustrated at the functional level as a combination of an "exclusive or" gate 708 and latch 710, is associated with each of the seven hundred and sixty-eight multiplexers 702 and serves to latch into the output bit map 706 the desired bit of the seven hundred sixty eight bits input to the multiplexer over the course of twenty four time slots. **That is, each 32 to 1 multiplexer selects one of 32 rails and the latching action of the control circuitry (that is, gate 708 and latch 710) selects the desired time slot of the 24 time slots. Consequently, the appropriate bit of 768 input bits, one of 32 in any one of the twenty four time-slots, may be selected for writing into a location within an output bit map 706.**

Since all seven hundred sixty eight input bits, one bit from each input channel, are sent to each of the selection blocks 701, any one bit may be sent to all the locations within the output bit map 706. That is, the switching core 700 may be used to broadcast data from any input channel to all the output channels. For example, if the selection block 701 points to rail 1, slot 1 in the output bit map 706 and its source, determined by a switch control map as previously discussed, is rail 8, slot 19 of an input bit map (not shown), the five bit control input to the multiplexer 702 could select rail 8 to appear at the

> output of the multiplexer 702 during all twenty four time slots. The enable circuit, functionally represented by the exclusive or circuit 708, would then activate the latch 710 only during incoming slot 19, thus selecting the bit appearing on rail 8 in time slot 19 for output to rail 1 time slot 1. In this illustrative embodiment, after 24 time slots, all the input bits have been switched to the appropriate location within the output bit map 706. The output bit map 706 may then be parallel loaded into another bitmap 712, which operates to buffer the output data and to allow the bitmap 706 to be loaded with output data for the next successive twenty four time slots." (See Applicants' Specification, page 12, line 27 through page 13 line 27). (emphasis added)

It is clearly evident from at least the disclosure of the Applicants' specification cited above, that the Applicants' claimed invention is capable of selecting any of the input bit packs from any of the rails in any of the time slots, and conveying said selected bit pack to any output data position within a combination of output data rails and time slots. The Applicants illustratively depict an input and output bit map for the display of input and output data. As the input data is organized in the input bit map, the Applicants teach how any of the available input data within the input bit map can be advantageously selected and conveyed to any output bit map (output data) position. The Applicants even further describe how one input data bit can be conveyed to all of the output data positions. Because any bit of 768 input bits, one of 32 in any one of the twenty four time-slots, may be selected, the input bits may be conveyed to any output data positions by conveying the input data bit to the desired output data position by, in one embodiment, when the desired rail and time slot is accessible. As such, the Applicants respectfully submit that at least claims 1, 5, 6, 11, 16, and 20 are supported by various passages in the Applicants' specification, and specifically within the passages of the specification recited above.

Therefore, the Applicants respectfully submit that claims 1, 5, 6, 11, 16, and 20 as they now stand, are definite, and hence fully satisfy the requirements of 35 U.S.C. § 112 and are patentable thereunder.

Furthermore, the Applicants respectfully submit that claims 2-4, 7-10, 12-15, 17-19 and 21-22, as they now stand, are also definite, and also fully satisfy the requirements of 35 U.S.C. § 112 and are patentable thereunder.

Conclusion

Thus the Applicants respectfully submit that all of the claims now present in the application, fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732) 530-9404 x1131 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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